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**IMPLEMENTATION OF PROGRAMMABLE ELECTRONIC SWITCHING SYSTEM
THROUGH VHDL**

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ABSTRACT

In this paper we are going to implement the programmable electronic switching system with the help of VHDL. The software we are using is XILINX version. There are three types of modeling used in VHDL, but here we are using behavior style of modeling. We have design different units: data memory, control memory input and output gates, counters, which performs their respective functions in order to connect input to the output subscriber.

KEYWORDS: Programmable Electronic Switching System Through Vhdl

INTRODUCTION TO VHDL

As digital systems have develop more and more complex, complete design of the system at the gate and flip flop level has become very tedious and the time consuming .For this reason , usage of hardware explanation languages in the digital design process continues to grow in very importance . An HDL (“HARDWARE DESCRIPTION LANGUAGE”) allows a digital system to be aimed and debugged at a higher level before conversion to gate flip-flop level.

The acronym VHDL stands for very high speed integrated Circuit hardware descriptive language .VHDL is the hardware descriptive language .VHDL is language for describing digital electronic systems

It VHDL is designed to meet out the number of requirements in a design process as follows:

- VHDL consents describing the purpose of the design behavioral manner with the provision for specifying its time explicitly .Also it allows descriptions of the design to be structured.
- VHDL is a type subtle to bits with a signal . An error is produced if a mismatch in the number of the associated signals is observed.
- VHDL indications to a top-down methodology in which a system is first specified at the higher level and verified using a simulator .The design can then be refined at the lower ranks for better and preferred results.

VHDL was deliberate to be technology autonomous and technology implementation part is occupied care of using implementation tools.

BASIC OF SWITCHING SYSTEM:

A major constituent of a switching system or the exchange is a input and output circuits called inlets and outlets. The primary function of the switching organization is to establish the path between inlet and the outlet. The hardware used is the switching network. If there are N inlets and M, outlets, when N=M the network is called regular network.

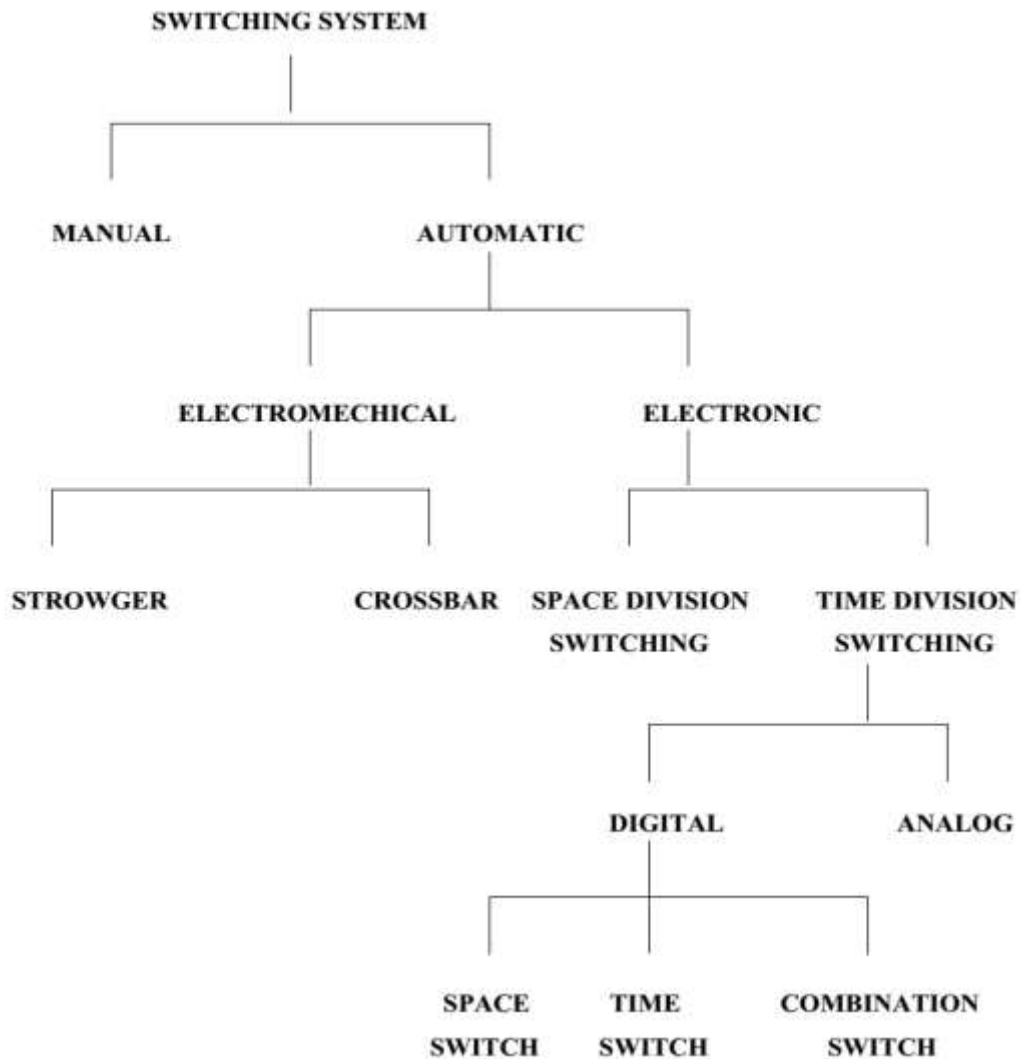


Figure 1:- Model of a switching network

SEQUENTIAL WRITE / RANDOM READ

There is an one to one communication between the inlets and the locations of the data memory. The control memory places cover the addresses of the inlets consistent to the outlets. The inlet addresses are read out from the control reminiscence in the second phase, a corresponding locations in the data recollection are retrieved and the data transferred to the outlets in the arrangement. Since any inlet may be associated to any of the outlets, the inlet discourses are randomly scattered in the control memory. Consequently, the read entrée to the data memory is random. Since the write admission to the data memory in the first phase proceeds sequentially and these read access in the second phase arbitrarily, the nomenclature sequential write / random read are used to describe this form of control.

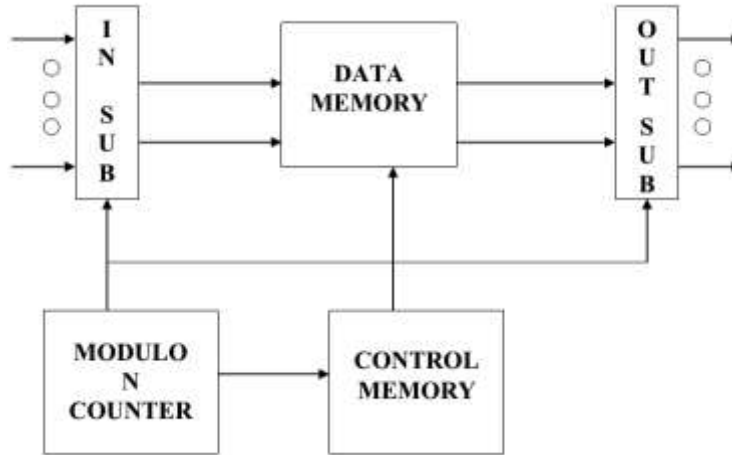


Figure 2:- Sequential write / Random read

RANDOM WRITE / SEQUENTIAL READ

The inlets are perused sequentially but the data are written into data memory randomly. Trendy the second phase of operation, the data recall is read out serially and the data is sent to the outlets sequentially. Nearby is no correspondence between the inlets and the control data reminiscence locations. But, there are one to one correspondence between the outlets and the switch memory locations. It may, however, be renowned that there is a one to one relationships between the inlets in the control memory locations.

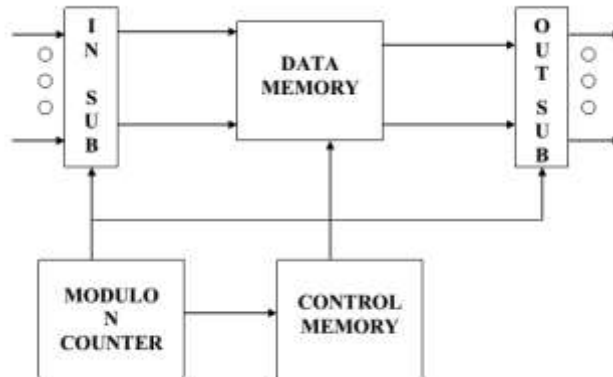


Figure 3:- Random write / Sequential read

E	I	D	D	D	S	S	S	X	X	X	X	X	X	X	X
		2	1	0	2	1	0								

1. 16 bit opcode
2. Interexchange: 8 users in each exchange can communicate with each other
3. Intraexchange: 8 users in one exchange can communicate with each other.
4. Data memory: 9bit of std_logic type (8 locations)
5. Control memory: 8 locations of integer type.
6. Caller id: 8 locations each of 3 bit

WORKING SPECIFICATIONS:

Phase 1: Input Subscribers in both the exchanges are scanned sequentially. It takes 8 clock cycles to scan 16 subscribers in order to know their status, that is they want to transmit or not. This is called a sequential scanning. The date to be transmitted is stored in data memory in sequential order. The information relating to the called

subscriber is stored in control memory in sequential order and caller id number is stored in the caller id memory in the same way. Thus we can say system is sequential write.

Phase 2: When all the scanning is finished the location of the data memory is read according to the corresponding location of the control memory. For example, if first location of data memory has data „I’bit and corresponding location in control memory is 2, this means that „d will be communicated to the 2nd user of the exchange, thus we can say the system is random read. To decide where the data will be communicated we use a bit in our op code as „I’ bit. If „I’bit =1, then it is interexchange, i.e. the read out data will be given to user of other exchange. Thus communication between the subscribers of two exchanges can be made possible and hence the name interexchange. If „I = 0, then it is called as intraexchange, i.e. the read out data, will be given to the user of the same exchange. Thus communication between subscribers of the same exchange is made possible, and hence the name Intraexchange.

FEATURES

- Dual way 32 user support
- Sequential Input Random Read
- Caller Id Facility
- Inter and Intra exchange
- 16 Bit data transfer
- In band Signalling
- Synchronization clock
- Reset features

SIMULATION RESULT

There are two exchange centers’ which taken as ‘din’ and ‘dout’. Our work has been implement for inter exchange and Intra exchange both. If we take ‘I’ is one then our design will work for inter exchange. If we take ‘I’ is zero then our design will work for Intra exchange. Our propose is depend on some more inputs clock, reset and enable. If reset is high then our design will not perform any function, all functions performed on low reset and positive edge of clock. If enable is zero then there is no exchange of data. Our exchanges are work on high enable bit.



Figure 4:- Simulation Result of phase 1

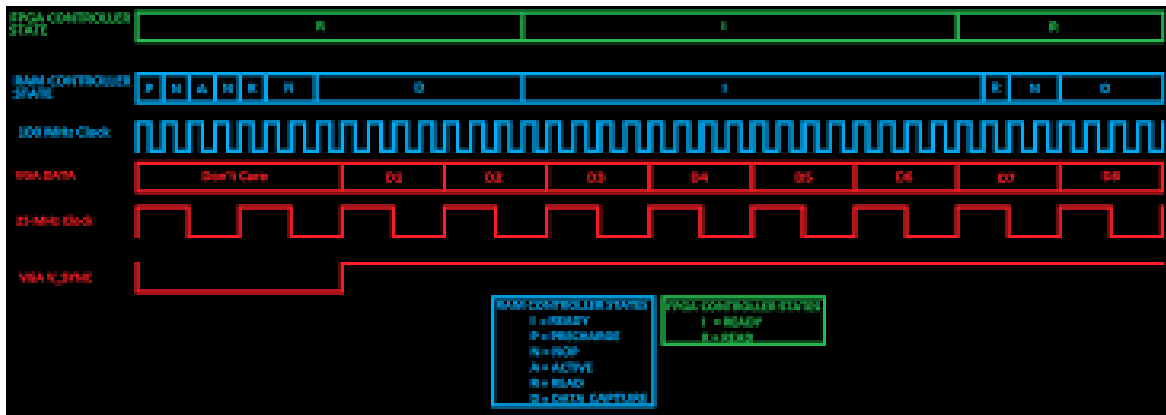


Figure 5:- Simulation Result of phase 2

CONCLUSION

We have shown above this generalized switching arrangement. The design of this switching structures are very complex and difficult to instrument in a limited period of time. That's why; in this dissertation we have intended the switching scheme with reduced number of blocks to achieve switching action.

Here we have considered one bit data transmission from effort subscriber to output subscriber. In that we have considered the programmable precise memory i.e. the addresses current in the different memory locations of regulator memory can be changed rendering to the desired essential of the user. For ease we have designed it for five numbers of subscribers.

Future Enhancement

We can design these switching system for N no. of subscribers having 8 bit data for every subscriber by considering the delay between input and output subscribers. In the VHDL programming we can upsurge the number of subscribers by using the KEYWORD known as "GENERIC" and for aggregate the number of bits we use the "MULTIDIMENSIONAL ARRAY".

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